Self-Aligned Fabrication of Graphene RF Transistors with T-Shaped Gate

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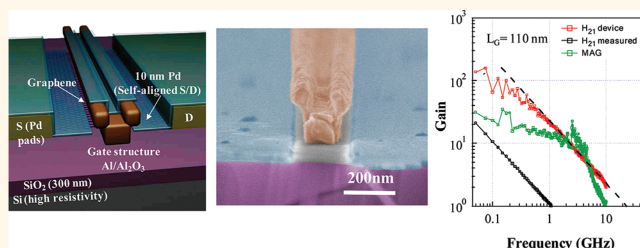
Graphene has attracted tremendous attention as a channel material for future electronic devices, due to its outstanding electronic properties.[1−4] In particular, high charge carrier mobility and saturation velocity, as well as strong carrier density modulation by electric field, result in very high transconductance for graphene field-effect transistors (FETs).[5−8] Moreover, single atomic layer thickness provides ultimate electrostatic geometry for scaling down channel lengths. Gate stacks, with equivalent oxide thickness (EOT) of 1.5 nm, which satisfy lateral gate scaling down to few nanometers, have been demonstrated for graphene FETs.[9] Significant advances have been made in the past for various graphene-based electronic devices and circuits;[10−17] however, most of the previous devices are not based on self-aligned transistor design and fabrication. In contrast, self-aligned transistor design has been the foundation for the silicon transistor and the semiconductor for the past several decades, as the self-aligned process uses a predefined polysilicon gate as a mask to form aligned source and drain automatically, which leads to minimized overlap between gate and source/drain, greatly simplified fabrication, and significantly improved device yield. As further evidence for the importance of self-aligned design, various self-aligned transistors have been reported for carbon nanotubes.[6,18−20] In spite of the utmost importance, self-aligned design and fabrication for graphene transistors have not been fully explored.

ABSTRACT



Exceptional electronic properties of graphene make it a promising candidate as a material for next generation electronics; however, self-aligned fabrication of graphene transistors has not been fully explored. In this paper, we present a scalable method for fabrication of self-aligned graphene transistors by defining a T-shaped gate on top of graphene, followed by self-aligned source and drain formation by depositing Pd with the T-gate as a shadow mask. This transistor design provides significant advantages such as elimination of misalignment, reduction of access resistance by minimizing ungated graphene, and reduced gate charging resistance. To achieve high-yield scalable fabrication, we have combined the use of large-area graphene synthesis by chemical vapor deposition, wafer-scale transfer, and e-beam lithography to deposit T-shaped top gates. The fabricated transistors with channel lengths in the range of 110−170 nm exhibited excellent performance with peak current density of 1.3 mA/μm and peak transconductance of 0.5 mS/μm, which is one of the highest transconductance values reported. In addition, the T-gate design enabled us to achieve graphene transistors with extrinsic current-gain cutoff frequency of 23 GHz and maximum oscillation frequency of 10 GHz. These results represent important steps toward self-aligned design of graphene transistors for various applications.

KEYWORDS: graphene · transistors · self-aligned fabrication · T-shaped gate · mushroom gate

In this paper, we report a scalable and reliable method for the fabrication of self-aligned graphene FETs. In order to optimize the design of the graphene FET, we propose a T-shaped top gate stack (or mushroom gate) patterned through standard lithographical methods. The T-shaped gate stack allows self-aligned source and drain formation by depositing Pd with the T-gate mask. We employed a simplified fabrication flow to obtain Al/Al_2O_3 T-shaped gate stack with a thin high-quality dielectric of equivalent oxide thickness down to 2.3 nm and gate lengths down to 100 nm. Combining this fabrication procedure with large-area graphene films grown by the chemical vapor deposition (CVD) method, we achieved scalable high-yield fabrication of a large number of graphene FETs on Si/SiO_2 substrates. The peak transconductance of the fabricated graphene FETs reaches 0.5 mS/μm, which is among the highest reported for graphene FETs. Actual transistor performance with current-gain cutoff frequency

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Received for review January 26, 2012 and accepted March 10, 2012.

Published online March 10, 2012
10.1021/nn300393c

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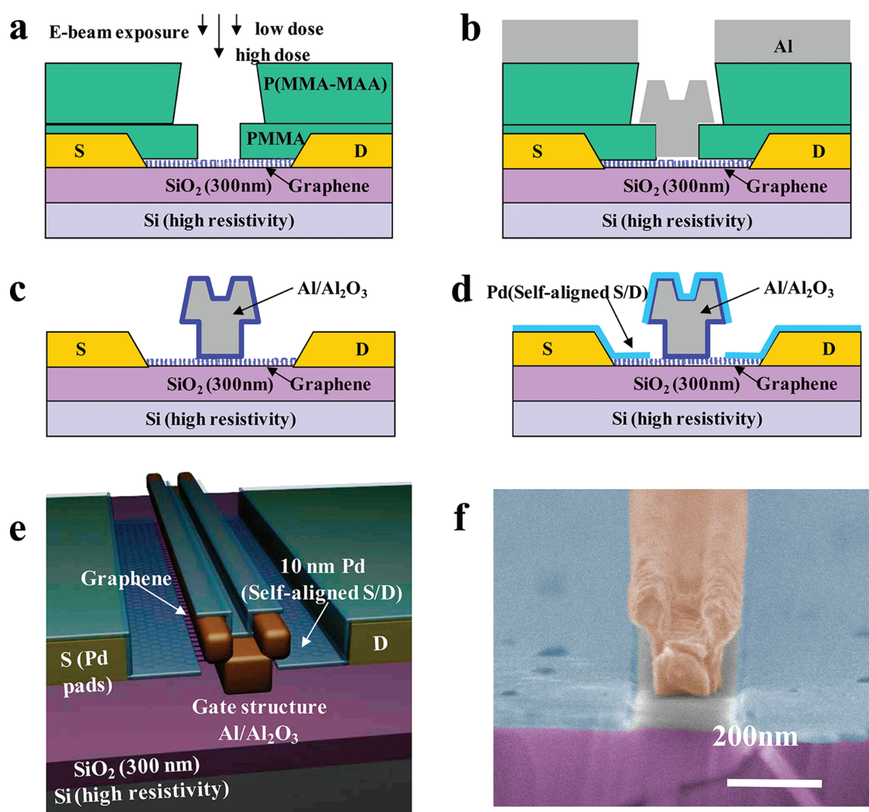

Figure 1. Fabrication flow and schematic diagram of self-aligned transistors based on the T-shaped gate stack. (a) Bilayer PMMA resist is exposed with high dose and adjacent low dose and developed. (b) Al film is deposited at normal direction to the substrate to form a T-shaped gate. (c) PMMA resist is removed, and Al gate is oxidized in air to form thin Al_2O_3 layer all around the gate, including the interface with graphene. (d) Thin Pd layer is deposited to form self-aligned source and drain contacts. Schematic image (e) and cross-section SEM image (f) of a complete self-aligned graphene transistor.

of 23 GHz and maximum oscillation frequency of 10 GHz is obtained for a transistor with a 110 nm gate length. The developed fabrication methods are highly scalable and suitable for further scaling down of device dimensions.

RESULTS AND DISCUSSION

Figure 1 illustrates the scalable fabrication of self-aligned graphene transistors based on the T-shaped gate. Details about the device fabrication process can be found in the Methods section. Large-area single-layer graphene films were synthesized and subsequently transferred onto highly resistive Si substrates with a 300 nm thick top SiO_2 layer, similarly to the previous reports.[17,21,22] A large number of active areas were first defined with standard lithographical methods by depositing metal pads and removing graphene films outside the channel. Graphene transistors were then fabricated using a scalable self-aligned approach based on a T-shaped gate stack. The self-aligned FET design and fabrication process flow are illustrated in Figure 1. In order to fabricate a T-shaped top gate stack, we used bilayer electron beam resist, and consequent development of the bilayer resist defined the pattern shown in Figure 1a. In addition, we have also employed the standard trilayer resist recipe for T-gate patterning, and similar results were achieved. The resulting side wall profile of the bilayer resist mask provided easy lift-off after aluminum (Al) film deposition, which left behind a T-shaped gate electrode (as shown in Figure 1c). The Al gate electrodes were then oxidized in air, forming a thin dielectric layer between graphene and the Al gate. The oxidation of Al at the interface with graphene was previously reported and attributed to the diffusion of oxygen due to weak physical interaction between the graphene surface and Al atoms.[23] Finally, a thin layer of palladium was deposited on top of the T-shaped gate, creating perfectly aligned source and drain electrodes for the graphene FET (Figure 1d). Figure 1f shows a cross-sectional SEM image of a complete device obtained after cleaving the substrate across the transistor channel. The metal source, drain, and gate electrodes were precisely aligned to each other and well-separated with short ungated graphene sections. This air gap leads to significant reduction of the parasitic fringe capacitance. The advantage of an air gap has been recently reported by Ding *et al.*[6] The separation distance is controlled by the length of the T-gate cap relative to the length of the T-gate base, which can be adjusted by the bilayer exposure recipe. We note that the standard T-gate technology used by the semiconductor industry usually employs the

trilayer resist recipe to define a very wide T-cap to reduce gate charging resistance; however, here we intentionally used a relatively narrow T-cap, as a wide T-cap can lead to large area of ungated graphene and thus high access resistance between the self-aligned source/drain and gated graphene. For such a T-gate with a narrow cap, we find that the bilayer resist recipe works very well and is simpler to process than the trilayer recipe.

In this report, we obtained channel lengths from 170 down to 110 nm, with the length of the ungated graphene sections about 20–40 nm. This geometry allows simultaneous reduction of the access resistance, fringe gate source, gate drain capacitance, and gate resistance. The length of the ungated sections can be further reduced by angle deposition of the source/drain metal film, which may lead to a trade-off between further reduction of the access resistance and increase of the parasitic fringe capacitance. On the basis of the calculation using the gate dimension and experimental measurements, we estimate the gate charging resistance to be ~1 Ω/μm of the gate width for a 100 nm long channel.

The above-mentioned fabrication method allowed us to achieve highly scalable and reliable fabrication of graphene transistors on complete Si wafers. CVD graphene synthesis on copper foils is readily extendable to very large areas by rolling up the foil.[21,22] In our case, we achieved graphene synthesis on copper foils as large as 12 in. in a 4 in. CVD chamber; furthermore, we successfully transferred the synthesized graphene to 12 in. Si wafers (Figure 2a). We carried out the fabrication of the T-gate graphene transistors for 2 in. wafer size due to the limitation of our lithography equipment. Figure 2b shows a 2 in. Si wafer with the fabricated graphene transistors. Figure 2c,d shows the top-view SEM images of a typical graphene T-gate transistor.

We first characterized the T-shaped Al/Al_2O_3 gate stack performance using electrical measurements. Figure 2e shows the conductance of a graphene FET as a function of the top gate voltage V_G and the back gate voltage V_{BG}. By comparing the shift of the charge neutrality point V_{CNP} (defined as the top gate voltage at the minimum conductance point), with the change of the back gate voltage V_{BG}, as shown in Figure 2f, we can find the top gate capacitance to be 130 times larger than the back gate capacitance.[5,9,24] For the 300 nm SiO_2 back gate dielectric, we estimate the back gate and top gate capacitances to be 11.8 and 1500 nF/cm^2, respectively. This capacitance corresponds to a dielectric with EOT of 2.3 nm, and hence we can estimate the thickness of the Al_2O_3 dielectric to be about 3–5 nm. The Al_2O_3 dielectric exhibits excellent insulator behavior with nearly 100% yield across all of the devices. According to the electrical measurement, the dielectric breakdown voltage is higher than 2.5 V, as shown in Figure 2g. This fabrication method provides a simple

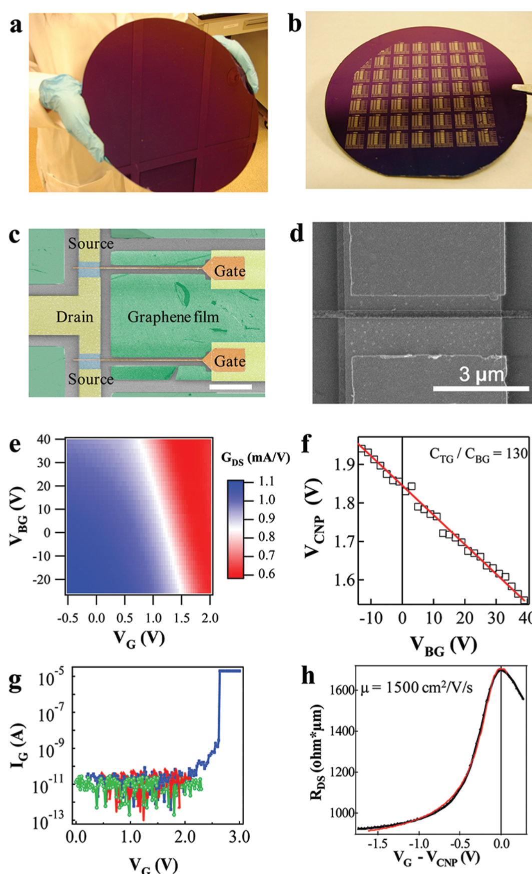

Figure 2. Electrical properties of the self-aligned graphene transistors. Photographs of 12 in. Si wafer with transferred large-area CVD-grown graphene (a) and 2 in. Si wafer with fabricated graphene transistors (b). (c) Artificial color SEM image of a self-aligned graphene transistor with the dual gate configuration, with the scale bar being 10 μm. (d) Zoomed-in SEM image of the transistor active area. (e) Two-dimensional plot of a graphene transistor conductance as a function of the top gate and back gate voltages. (f) Top gate voltage at the charge neutrality point *versus* back gate voltage. The slope of the lines gives the ratio of top gate dielectric capacitance to the bottom gate dielectric capacitance equal to 130. (g) Gate leakage current of few graphene transistors; both source and drain are grounded. Dielectric breakdown voltage is higher than 2.5 V. (h) Scaled resistance of a graphene transistor *versus* top gate voltage. Black curve is the experimental result, and red curve is the model fitting.

and reliable method to obtain gate stacks with a high-quality dielectric for graphene devices. The mobility μ and contact resistance R_C of a graphene FET can be extracted by fitting the source–drain linear resistance R_{DS} with the formula $R_{DS}W = 2R_CW + L/[\mu e(n_0^2 + n^2)^{1/2}]$, where L is the channel length, W is the channel width, n_0 is the residual carrier density, and n is the carrier density due to top gate modulation.[6,24,25] Figure 2h shows the measurement and the fit of the resistance of a graphene FET with 170 nm channel length. We find the hole mobility equal to 1500 cm^2/V·s, residual carrier concentration n_0 of 5×10^{11} cm^{-2}, and scaled contact resistance R_CW of about 400 Ω·μm. These parameters are not as good as the values of exfoliated graphene but comparable to the values for other graphene FETs.

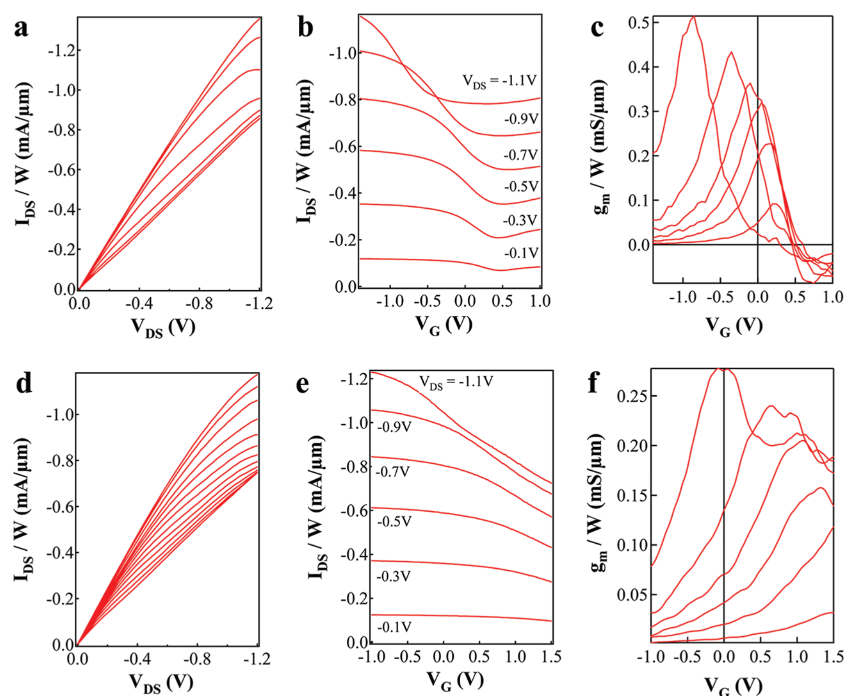

Figure 3. DC output and transfer characteristics of two graphene transistors of 170 nm (a–c) and 110 nm (d–f) channel length. Scaled transistor current (I_{DS}/W) *vs* drain voltage (V_{DS}) (a) and gate voltage (b); and scaled transconductance (g_m/W) *vs* gate voltage (V_G) (c) for the transistor with 170 nm channel length. Scaled transistor current (I_{DS}/W) *vs* drain voltage (V_{DS}) (a) and gate voltage (b); and scaled transconductance (g_m/W) *vs* gate voltage (V_G) (c) for the transistor with 110 nm channel length. Back gate (substrate) voltage was kept constant and equal to 0 V for all plots.

Figure 3 shows the output and transfer characteristics of two graphene FETs with a channel length of 170 nm (Figure 3a–c) and 110 nm (Figure 3d–f), respectively. For the output characteristics (Figure 3a), the drain voltage sweeps from 0 to −1.2 V, with the top gate voltage step of +0.2 V starting from −1.6 V for the top curve. The transistors exhibit large drive current densities up to 1.3 mA/μm and ~50% gate modulation, as well as appreciable current saturation with output conductance as low as 0.2 mS/μm. The transfer curves (Figure 3b) and transconductance curves (Figure 3c) are obtained with gate voltage swept from −1.5 to 1 V, and the drain voltage varied from −1.1 to −0.1 V (in −0.2 V steps) from the top to bottom curves. The saturation in $I_d - V_{ds}$ curves at intermediate gate voltages shown in Figure 3a is consistent with previous reports[17,24] and is believed to be a result of the presence of the minimal density point close to the drain under the right combination of gate voltage and drain voltage.[24] A peak scaled transconductance g_m/W up to 0.5 mS/μm was achieved for the 170 nm device. From comparison, the on/off current ratio and transconductance of the transistors with 110 nm channel length are lower than those of the transistors with 170 nm channel length. For example, the peak transconductance for the 110 nm channel length is measured to be 0.27 mS/μm (Figure 3f). Similar channel dependence was reported before.[14] One possible reason is that the significant contact resistance in our devices has more pronounced influence on the performance of short channel transistors than long channel transistors. Moreover, quasi-ballistic transport and strong interband tunneling in graphene may exert influence on short channel transistors, as suggested before.[14]

We further characterized the high-frequency performance of the graphene transistors by standard on-chip S-parameter measurements with a vector network analyzer over the frequency range of 0.05 to 10 GHz. The measurements were first calibrated to the probe tips using an off-chip calibration substrate by a standard short-open-load-through (SOLT) procedure. A de-embedding procedure was then used to eliminate the effect of the co-planar waveguide pads on the RF performance by measuring on-chip "open" and "short" test structures. The open test structure consisted of only large photolithography-defined pads outside the active area of the transistors, while the short test structure has additional metal film shorting the gate source and drain source pads (Figure S3, Supporting Information). The S-parameters after this de-embedding procedure are determined by the graphene transistor channel, top gate electrode with gate interconnect, and ~1 μm long metal source and drain electrodes outside the channel. We call the de-embedded results the "device" performance because it is the performance that is accessible for actual integrated on-chip circuits. Figure 4 shows the current gain (H_{21}) and maximum available gain (MAG) for two transistors with channel lengths of 170 nm (Figure 4a) and 110 nm (Figure 4b). The measured and device

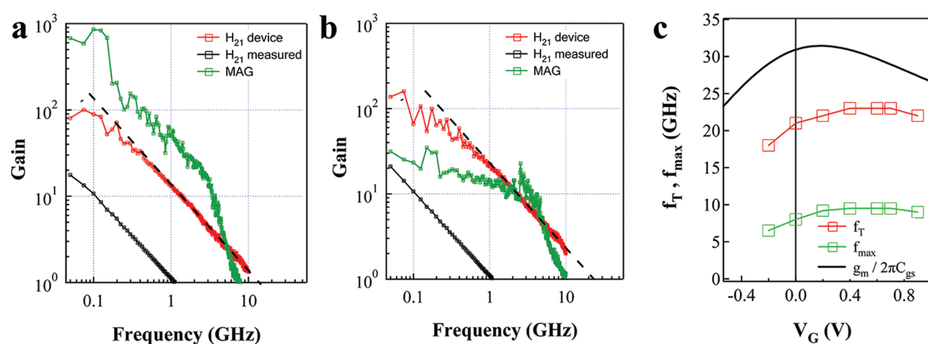

Figure 4. RF performance of graphene transistors. (a,b) Current gain (H_{21}) before (black line) and after (red line) the de-embedding procedure and maximum available gain (MAG) (green line) for two graphene transistors with 170 nm channel length (a) and 110 nm channel length (b). (c) Plot of f_T, f_{max}, and intrinsic gate delay ($g_m/2\pi C_g$), evaluated from DC measurements, *versus* gate bias (V_G) for the 110 nm transistor.

current gains are the results before and after the de-embedding procedure, respectively. A current-gain cutoff frequency (f_T) of 15 GHz and maximum oscillation frequency (f_{max}) of 8 GHz are obtained for the 170 nm device, and f_T of 23 GHz and f_{max} of 10 GHz are obtained for the 110 nm device. Altogether, we have fabricated 20 devices, and all of the devices showed f_T in the range of 5−25 GHz.

The highest achievable current-gain cutoff frequency in a FET is limited by the intrinsic gate delay and given by $f_T = g_m/2\pi C_g$, where C_g is the total gate capacitance. Figure 4c shows the comparison between the intrinsic gate delay frequency, which is evaluated from the DC measurements of the transconductance and gate capacitance, and the device current-gain cutoff frequency and maximum oscillation frequency from the RF measurements. We find the device current-gain cutoff frequency to be relatively close to the intrinsic gate delay frequency value, which shows that the parasitic effects of the T-shaped gate transistor play a small role and justifies the improved device design.

Owing to the T-gate design, our transistors exhibit excellent microwave power gain with f_{max} up to 10 GHz, which is comparable to the best reported values.[8,17] The current-gain cutoff frequency (f_T) of our transistors, however, is lower than some of the reported values in literature.[16,17,26] We note that the main factors limiting the performance may include graphene−metal contact resistance, inhomogeneity of carrier concentration due to impurities, corrugation, and wrinkles in the graphene channel, and quality of the graphene/dielectric interface. Further improvement of both f_T and f_{max} of the graphene FETs can be achieved by using the T-gate transistor design with a metal−graphene junction and transferred graphene quality improved.

CONCLUSION

In summary, we have developed a scalable self-aligned fabrication method utilizing a T-shaped gate structure to fabricate graphene transistors. By using the T-shaped gate design, we successfully scaled the channel length of graphene transistor down to 110 nm with good alignment. The graphene transistors with channel lengths in the range of 110−170 nm exhibit excellent on-chip device performance with a peak transconductance up to 0.5 mS/μm. The developed fabrication method is highly scalable and reliable, which allows the fabrication of a large number of self-aligned graphene transistors with high yield. In addition, while the work reported above deals with analog RF transistors, our self-aligned T-gate fabrication can be combined with patterned or assembled graphene ribbons with a band gap to produce high-performance transistors with high on/off ratio for digital electronics. Moreover, this simple fabrication approach to obtain a self-aligned transistor can work as an excellent platform for realization of highly scaled transistors based on other carbon nanostructures, such as carbon nanotubes and graphene nanoribbons. Our work represents an important step toward practical implementation of graphene devices and circuits.

METHODS

Self-Aligned T-Gate Graphene RF Transistor Fabrication. Large-area single-layer graphene films were synthesized on copper foils by a low-pressure CVD method and subsequently transferred onto a highly resistive silicon wafer ($\rho > 5$ k$\Omega \cdot$cm) with a 300 nm thick top SiO_2 layer. Titanium/palladium (0.5/50 nm) probing pads are first patterned using a contact aligner and lift-off process. After this, bilayer electron beam resist, with the top layer, the copolymer of methyl methacrylate and methacrylic acid P(MMA-MAA), being more sensitive than the bottom layer, polymethyl methacrylate (PMMA) with 950k molecular weight, is used to fabricate T-shaped top gate stack. The bilayer resist was exposed with high dose at the gate position center and low dose at the adjacent area in the same exposure run. After the deposition of aluminum film (140 nm), a standard lift-off process produces the T-shaped gate stack. The Al gate electrodes were then oxidized in air, forming a thin dielectric layer between graphene and the Al gate. Finally, a thin layer of palladium

(12 nm) was deposited on top of the T-shaped gate to create aligned source and drain electrodes for the graphene FET.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. We would like to acknowledge the collaboration of this research with King Abdulaziz City for Science and Technology (KACST) and Office of Naval Research sponsorship. We also thank Prof. Kang L. Wang, Dr. Kosmas Galatsis, Dr. Hani Enaya, Alborz Jooyaie, and Mingqiang Bao for fruitful discussions.

Supporting Information Available: Details of the experimental methods and supporting figures. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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